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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,642	03/15/2005	Mitsuhiro Yuasa	101249.55749US	2849

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EXAMINER	
DURBIN, MICHAEL H	

ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
09/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,642	YUASA, MITSUHIRO	
	Examiner	Art Unit	
	Michael Durbin	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133): Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *3,12-15 and 17-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-11 and 16* is/are rejected.

7)☐ Claim(s) *1 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/09/06, 08/08/06, 12/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 2, 12-15, and 17-23 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention and species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 08/20/2007.

Claim Objections

2. Claims 1 and 16 are objected to because of the following informalities:

For claim 1, the preamble recites "a MEMS array." It is unclear how the device, when the switching elements are semiconductor switches, how the device can be considered a MEMS array. There are no limitations reciting any part of a MEMS structure in the elected claims. Applicant's specification discloses two embodiments: one with transistor switches and the other with MEMS switches. The examiner suggests that this recitation is removed from the preamble of the claims.

Further, the recitation of a MEMS device has not been given patentable weight in any of the claims because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural

limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

For claim 16, the Examiner suggests that "built in" is amended to read "built therein" to correct a mistake in the sentence structure.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

3. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "a MEMS array" in the elected claims is used by the claim to mean "an array comprising passive components connected through an network of transistors", while the accepted meaning is "an array of electro-mechanical devices." The term is indefinite because the specification does not clearly redefine the term. A MEMS array must contain mechanical parts that are driven electronically.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Wallace et al. (US Patent 6,271,728) (hereinafter Wallace).**

6. Regarding claims 1 and 2, figure 11 of Wallace discloses a device array characterized by being provided with pluralities of various types of elements (elements such as capacitors and resistors provided in low- and high- pass filters [col. 8, lines13.– col. 10, line 7]) for each type and switches (semiconductor transistors T1, T2, T3, etc. as seen in fig. 11; [col. 8, line 55- col. 10, line 7) for connecting said elements and by enabling the elements to be freely interconnected (the array is a network of phase shifter stages).

As mentioned above under the Claim Objections heading, the recitation of a MEMS device has not been given patentable weight in any of the claims because the recitation occurs in the preamble.

7. **Claims 4 – 11 and 16 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Wallace, in view of Lucas et al. (US 6,287,951 B1).**

8. Regarding claim 4, Wallace discloses that the device is a fully integrated chipset (col. 3, lines 39-55). It follows that the device will have a semiconductor substrate for the formation of transistors and a conductive interconnect layer to interconnect devices. These limitations are inherent to all integrated semiconductor devices. If Applicant can show that this limitation is not inherent to every integrated semiconductor device, then it

would at least been obvious in order to form a fully integrated device with know techniques. Lucas teaches the use of a device comprising an integrated circuit comprising transistors formed in the substrate (also in the first interconnect level as seen in figure) along with a plurality of elements formed in an interconnect layer (the interconnects are at least resistors). It would have been obvious to modify Wallace with the teachings of Lucas to create a fully integrated device of for reduced manufacturing costs and reduced size.

9. Further for claims 4 and 8, Wallace does not explicitly state that the circuit as seen in fig. 11 has the elements formed in an interconnect layer. It would have at least been obvious to for the elements in an interconnect layer for the purpose of integrating the device. Also, because the gate stacks of the switches reside in the interconnect level with level contacts the switches, the switches themselves are considered to be provided in the interconnect layer due to this proximity.

10. Regarding claim 5 and 9, Wallace discloses that all necessary parts are integrated into the chipset (col. 3, lines 39-55) and that the drive parts are to be provided (col. 8, lines 9-12).

11. Regarding claim 6 and 10, Wallace discloses that the device is capable of filtering an input wave (col. 8, lines 13-24).

12. Regarding claim 7 and 11, all semiconductor circuits have three-dimensional structures, as they exist in three-dimensions.

13. Regarding claim 16, all the devices reside in the same package as all the devices are integrated into the same chipset (col. 3, lines 39-55).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Durbin whose telephone number is (571) 272-9766. The examiner can normally be reached on M-T 7:30-5; 1st Fri. of biweek off, 2nd 7:30-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Durbin
Examiner
Art Unit 2815

MHD

Matthew C. Landau
9/11/07